BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application:	G.R. Mohan Rao
Serial No.:	10/665,906
Filed:	September 18, 2003
Art Unit:	2188
Examiner:	Portka, Gary J.
Title:	MEMORIES FOR ELECTRONIC SYSTEMS

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Silicon Aquarius Incorporated.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-21 are pending in the Application. Claims 1-21 stand rejected. Claims 1-21 are appealed.

IV. STATUS OF AMENDMENTS

Appellant has not submitted any amendments following receipt of the final office action with a mailing date of July 26, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1:

In one embodiment of the present invention, a switch comprises a plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of the ports. Specification, page 9, paragraph [0030]; Figure 1A, elements 100, 102, ports 1-8. The shared memory comprises an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. Specification, pages 10-17, paragraphs [0035-0048]; Figure 2A, element 202. The shared memory may further comprise circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined word-width during a first time period and for reading the selected data as a word of the predetermined word-width from the selected row during a second time period for output at the second one of the ports. Specification, pages 10-17, paragraphs [0035-0048].

Independent Claim 8:

In one embodiment of the present invention, a shared-memory switch comprises a plurality of ports for exchanging data between external devices associated with each of the ports. Specification, pages 9-10, paragraphs [0030-0034]; Figure 1, elements 100, ports 1-8. The switch may further comprise a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width and for converting single data words of the predetermined width being output from the switch into a stream of data words. Specification, pages 9-10, paragraphs [0030-0034]; Figure 1, elements

103a-h. The switch may further comprise a shared-memory for effectuating a transfer of data from a first one of the ports to a second one of the ports through corresponding ones of the buffers, the shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of the predetermined width and circuitry for selecting a row in response to a received address. Specification, pages 9-17, paragraphs [0030-0048]; Figure 1, element 102, 103a-h, ports 1-8; Figure 2A, elements 201, 202. The switch may further comprise a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data to a corresponding one of the banks. Specification, pages 10-17, paragraphs [0035-0048]; Figure 2A, elements 201, 210. The switch may further comprise a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of the banks. Specification, pages 10-17, paragraphs [0035-0048]; Figure 2A, elements 201, 211.

Independent Claim 16:

In one embodiment of the present invention, a digital information system comprises first and second resources operable to exchange data in a selected digital format. Specification, page 19, paragraphs [0055-0056]; Figure 5, elements 501-507. The system may further comprise a digital switch comprising first and second ports for selectively coupling the first and second resources. Specification, pages 9-10, paragraphs [0030-0034]; Figure 1A, elements 100, ports 1-8. The digital switch may further comprise a shared memory for enabling the exchange of data between the first and second ports as words of a predetermined word-width. Specification, pages 9-10, paragraphs [0030-0034]; Figure 1A, element 102. The shared memory may comprise an array of memory cells arranged as a plurality of rows and a single column having a width equal to the predetermined word-width. Specification, pages 10-17, paragraphs [0035-0048]; Figure 2A, element 202. The shared memory may further comprise circuitry for writing a selected data word presented at the first one of the ports to a selected row in the array during a first time period and for reading the selected data

word from the selected row during a second time period to the second one of the ports. Specification, pages 10-17, paragraphs [0035-0048].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-3, 5-8, 10-17 and 20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Mathur (U.S. Patent No. 6,424,658).

B. Claims 1-3, 7, 16-17 and 20-21 stand rejected under 35 U.S.C. §102(e) as being anticipated by Curtis et al. (U.S. Patent No. 6,925,086) (hereinafter "Curtis").

C. Claims 4, 9 and 18-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mathur, or alternatively, over Curtis.

D. Claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Mathur.

VII. ARGUMENT

A. Claims 1-3, 5-8, 10-17 and 20 are not properly rejected under 35 U.S.C. §102(b) as being anticipated by Mathur.

The Examiner has rejected claims 1-3, 5-8, 10-17 and 20 under 35 U.S.C. §102(b) as being anticipated by Mathur. Office Action (7/26/2006), page 2. Appellant respectfully traverses these rejections for at least the reasons stated below.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

1. Claims 1 and 16 are not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "an array of

memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16. The Examiner cites packets 3 and 6 in Figure 9 as well as column 1 in Figure 9 of Mathur as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 2. Appellant respectfully traverses.

Mathur instead discloses that in the example of Figure 9, the packet memory is divided into several regions, one for each input port. Column 11, lines 37-38. Mathur further discloses that the output ports are not assigned any memory space. Column 11, lines 38-39. Mathur further discloses that the region for port A includes rows 1, 2, 3, 4, while the region for port C contains rows 34, 35, 36, 37. Column 11, lines 39-41. Mathur further discloses that packet 1 received by port A is written into row 1. Column 11, line 44. Mathur further discloses that since this is a small packet of 64 bytes, it occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Mathur further discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50. Hence, as illustrated in Figure 9, Mathur discloses dividing the packet memory into regions corresponding to each input port. Each region includes multiple rows that are allocated to store data from a particular input port. Further, each row includes 48 columns in which all or a portion of the columns may be used to store the data received from the associated input port.

There is no language in the passages that describe Figure 9 that discloses a shared memory that includes an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. Instead, Mathur discloses 48 columns for each row where all or a portion of the columns may be used to store the data received from the associated input port. Thus, Mathur does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner states:

> There is no requirement to interpret the claimed 'column' to be equal to what Mathur calls a column as in Mathur Fig. 9. Applicant has not precisely defined what a 'word' as claimed. If a maximum packet length is considered a word width, packets 3 and 6 extend the length of the row, and thus COL 1 to COL 48 may be considered a single column of word width 256x48 in Mathur Fig. 9 (it is further noted that there is no claimed requirement that each row of the column be fully written with an entire word width). Alternatively as stated hereinabove, the recited array may be considered simply the COL 1 of Fig. 9 with word width equal to half the packet length of, for example, packets 1 or 7, or the COL 1 plus the COL 2 with word width equal to the packet length of packets 1 or 7. Office Action (7/26/2006), page 6.

Appellant respectfully asserts that the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that columns 1-48 of Figure 9 of Mathur is interpreted as a single column having a width equal to a predetermined word-width. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that columns 1-48 of Figure 9 of Mathur is interpreted as a single column having a width equal to a predetermined word-width, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1 and 16. M.P.E.P. §2131.

Further, the Examiner has not provided any language in Mathur that would cause one of ordinary skill in the art to interpret columns 1-48 of Mathur as being a single column In fact, column 11, lines 11-57 of Mathur specifically uses language that interprets columns 1-48 as being separate 48 columns.

Further, even though Appellant may not have specifically defined the term "word" in the Specification, this does not allow the Examiner to interpret "column" to mean anything. The pending claims must be given their broadest reasonable

interpretation consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2d 1664, 1667 (Fed. Cir. 2000); M.P.E.P. §2111. The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. §2111. Since the Examiner has not provided a reasonable interpretation consistent with the specification or consistent with the interpretation that those skilled in the art would reach, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1 and 16. M.P.E.P. §2111.

Further, the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that column 1 or columns 1 and 2 of Figure 9 of Mathur can be interpreted as a single column having a width equal to a predetermined word-width. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that column 1 or columns 1 and 2 of Figure 9 of Mathur can be interpreted as a single column having a width equal to a predetermined word-width, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1 and 16. M.P.E.P. §2131.

Appellant further asserts that Mathur does not disclose "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16. The Examiner cites column 1, line 55 – column 2, line 11; column 4, lines 31-44; column 5, lines 56-61; column 11, lines 44-56 and Figures 6 and 7 of Mathur as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 3. Appellant respectfully traverses.

Mathur instead discloses network switches have been used to connect LANs to other LANs, and even to connect network elements within a single LAN. Column 1, lines 55-57. Mathur further discloses that in further aspects the port controller for the input port writes an entire packet to a row of the embedded packet memory without interruption by other port controllers. Column 4, lines 31-33. Mathur additionally discloses that when packets are aligned to DRAM pages, the inventor has realized that only the DRAM row address where the packet is stored needs to be sent to the receiving port. Column 5, lines 56-58. Furthermore, Mathur discloses that since this is a small packet of 64 bytes, it occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Additionally, Mathur discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50.

There is no language in the cited passages that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width. Neither is there any language in the cited passages that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width during a first time period. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period for output at the second one of the ports. Thus, Mathur does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Mathur discloses the above-cited claim limitation without providing any evidence. Office Action (7/26/2006), page 7. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 1 and 16. M.P.E.P. §2131.

2. Claim 8 is not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words" as recited in claim 8. The Examiner cites column 6, lines 36-65 of Mathur as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 3. Appellant respectfully traverses and asserts that Mathur instead discloses that port A logic and port B logic are bi-directional, each having a receive first-in-first-out FIFO and a transmit FIFO that connects to a twisted pair through physical-layer transceivers. Column 6, lines 33-36. Hence, Mathur discloses that the ports include FIFO buffers. There is no language in the cited passage that discloses a buffer associated with each of the ports. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width and for converting single data words of the predetermined width being output from the switch into a stream of data words. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by

Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Mathur discloses the above-cited claim limitation without providing any evidence. Office Action (7/26/2006), page 7. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claim 8. M.P.E.P. §2131.

Appellant further asserts that Mathur does not disclose "a shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a said row in response to a received address" as recited in claim 8. The Examiner cites packets 3 and 6 in Figure 9 as well as column 1 in Figure 9 of Mathur as disclosing the above-cited claim limitation. Office Action (7/26/2006), pages 2-3. Appellant respectfully traverses.

Mathur instead discloses that in the example of Figure 9, the packet memory is divided into several regions, one for each input port. Column 11, lines 37-38. Mathur further discloses that the output ports are not assigned any memory space. Column 11, lines 38-39. Mathur further discloses that the region for port A includes rows 1, 2, 3, 4, while the region for port C contains rows 34, 35, 36, 37. Column 11, lines 39-41. Mathur further discloses that packet 1 received by port A is written into row 1. Column 11, line 44. Mathur further discloses that since this is a small packet of 64 bytes, it occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Mathur further discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50. Hence, as illustrated in Figure 9, Mathur discloses dividing the packet memory into regions

corresponding to each input port. Each region includes multiple rows that are allocated to store data from a particular input port. Further, each row includes 48 columns in which all or a portion of the columns may be used to store the data received from the associated input port.

There is no language in the cited passages that discloses a shared-memory for effectuating a transfer of data from a first one of the ports to a second one of the ports through corresponding ones of the buffers. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks[1]. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of the predetermined width and circuitry for selecting a row in response to a received address. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner asserts that "Port A" and "Port B" in Figure 9 of Mathur is interpreted as banks. Office Action (7/26/2006), page 7. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that ports of Figure 9 of Mathur can be interpreted as banks. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that ports of Figure 9 of Mathur can be interpreted as banks, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

[1] The Examiner appears to be asserting that each row of the packet memory is considered to be a bank. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that each row of the packet memory, as disclosed in Mathur, is a bank. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that it would have been recognized by persons of ordinary skill that each row of the packet

Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 8. M.P.E.P. §2131.

Appellant further asserts that Mathur does not disclose "a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks" as recited in claim 8. The Examiner cites column 9, lines 8-25 of Mathur as disclosing the above-cited claim limitations. Office Action (7/26/2006), page 3. Appellant respectfully traverses and asserts that Mathur instead discloses that the input-port table is a memory allocation table with one entry for each row of the packet memory allocated to the port. Column 9, lines 8-10. Mathur further discloses that each entry contains the row address and a free/busy bit. Column 9, line 10. Hence, Mathur discloses a single table that contains entries containing row addresses. There is no language in the cited passage that discloses a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data. Neither is there any language in the cited passage that discloses a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data to a corresponding one of the banks. Neither is there any language in the cited passage that discloses a plurality of used address tables each for maintaining a queue of addresses for reading. Neither is there any language in the cited passage that discloses a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of the banks. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

3. Claims 2-3 and 5-6 are not anticipated by Mathur for at least the reasons that claim 1 is not anticipated by Mathur.

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memory, as disclosed in Mathur, is a bank. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

Claims 2-3 and 5-6 each recite combinations of features of independent claim 1, and thus claims 2-3 and 5-6 are not anticipated by Mathur for at least the reasons that claim 1 is not anticipated by Mathur.

4. Claims 10-15 are not anticipated by Mathur for at least the reasons that claim 8 is not anticipated by Mathur.

Claims 10-15 each recite combinations of features of independent claim 8, and thus claims 10-15 are not anticipated by Mathur for at least the reasons that claim 8 is not anticipated by Mathur.

5. Claims 17 and 20 are not anticipated by Mathur for at least the reasons that claim 16 is not anticipated by Mathur.

Claims 17 and 20 each recite combinations of features of independent claim 16, and thus claims 17 and 20 are not anticipated by Mathur for at least the reasons that claim 16 is not anticipated by Mathur.

6. Claims 2 and 17 are not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17. The Examiner cites column 6, lines 36-65 of Mathur as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 3. Appellant respectfully traverses and asserts that Mathur instead discloses that port A logic and port B logic are bi-directional, each having a receive first-in-first-out FIFO and a transmit FIFO that connects to a twisted pair through physical-layer transceivers. Column 6, lines 33-36. Hence, Mathur discloses that the ports includes FIFO buffers. However, claims 2 and 17 do not recite a port that comprises a buffer. Instead, claims 2 and 17 recite a buffer associated with each port. Neither is there any language in the cited passage that discloses a buffer associated with each port for converting words of data from an initial bit-width to the predetermined bit width. Thus, Mathur does not disclose all of

the limitations of claims 2 and 17, and thus claims 2 and 17 are not anticipated by Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Mathur discloses the above-cited claim limitation without providing any evidence. Office Action (7/26/2006), page 7. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 2 and 17. M.P.E.P. §2131.

7. Claim 3 is not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead" as recited in claim 3. The Examiner has not specifically addressed this claim limitation. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 3. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to assert that the above-cited claim limitation is well known in the art. Office Action (7/26/2006), page 7. Appellant respectfully traverses that the above-cited claim limitation is well known in the art. The Examiner has not provided any evidence that the above-cited claim limitation is well known in the art. The Examiner is instead relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of anticipation. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P.

§2131. Hence, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 3. *Id.*

8. Claim 6 is not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "a used addressed table for storing addresses already used for writing data to selected rows in said array" as recited in claim 6. The Examiner cites column 9, lines 8-25 and column 10, lines 1-15 of Mathur as disclosing the above-cited claim limitations. Office Action (7/26/2006), page 3. Appellant respectfully traverses and asserts that Mathur instead discloses that the input-port table is a memory allocation table with one entry for each row of the packet memory allocated to the port. Column 9, lines 8-10. Mathur further discloses that each entry contains the row address and a free/busy bit. Column 9, line 10. Mathur further discloses that Figure 7 is a diagram of the read controller for an output port that reads the packet from the embedded DRAM packet memory. Column 10, lines 2-4. Hence, Mathur discloses a table that contains entries containing row addresses. There is no language in the cited passage that discloses a table for storing addresses already used for writing data. Neither is there any language in the cited passage that discloses a table for storing addresses already used for writing data to selected rows in the array. Thus, Mathur does not disclose all of the limitations of claim 6, and thus claim 6 is not anticipated by Mathur. M.P.E.P. §2131.

9. Claim 10 is not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "wherein each of said plurality of available address tables comprises a first-in-first-out memory" as recited in claim 10. The Examiner states that "the input port table in Mathur operates as a FIFO as recited." Office Action (7/26/2006), page 3. Appellant respectfully

traverses and asserts that there is no language in Mathur[2] that discloses that input-port table (element 60) in Mathur comprises a FIFO memory as asserted by the Examiner. Thus, Mathur does not disclose all of the limitations of claim 10, and thus claim 10 is not anticipated by Mathur. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner states that the counter of Figure 6 operates by counting to the end of a packet. Office Action (7/26/2006), page 7. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a counter of Figure 6 of Mathur discloses that each of the plurality of available address tables comprises a first-in-first-out memory. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a counter of Figure 6 of Mathur discloses that each of the plurality of available address tables comprises a first-in-first-out memory, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 10. M.P.E.P. §2131.

10. Claims 11-15 are not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not the limitations of claims 11-15. The Examiner has not specifically addressed these claim limitations. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the claim limitations of claims 11-15, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 11-15. M.P.E.P. §2131.

[2] Column 9, lines 1-16 of Mathur discuss the input port table.

In response to Appellant's above argument, the Examiner appears to simply assert that Mathur discloses the claim limitations of claims 11-15 without providing any evidence. Office Action (7/26/2006), pages 7-8. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 11-15. M.P.E.P. §2131.

11. Claim 20 is not anticipated by Mathur.

Appellant respectfully asserts that Mathur does not disclose "wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment" as recited in claim 20. The Examiner has not specifically addressed this claim limitation. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 20. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Mathur discloses the claim limitations of claim 20 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claim 20. M.P.E.P. §2131.

B. Claims 1-3, 7, 16-17 and 20-21 are not properly rejected under 35 U.S.C. §102(e) as being anticipated by Curtis.

The Examiner has rejected claims 1-3, 7, 16-17 and 20-21 under 35 U.S.C. §102(e) as being anticipated by Curtis. Office Action (7/26/2006), page 4. Appellant respectfully traverses these rejections for at least the reasons stated below.

As stated above, for a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

1. Claims 1 and 16 are not anticipated by Curtis.

Appellant respectfully asserts that Curtis does not disclose "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16. The Examiner cites column 1, lines 45-52; column 4, lines 19-29 and Figures 1, 3 and 6 of Curtis as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 4. Appellant respectfully traverses and asserts that Curtis instead discloses a packet memory system that includes a memory cell array for storing a predefined number of packets. Column 1, lines 46-48. Curtis further discloses that each packet includes a pre-determined number of segments. Column 1, lines 48-49. Curtis further discloses that each of the segments defines a starting point of a memory access. Column 1, lines 49-50. Curtis further discloses a cache line packet broken into four segments A, B, C and D. Column 4, lines 19-21. Curtis further discloses a memory cell array (element 102) that allows a device to read or write one cell after another and allows it to stop a burst at any point along the way. Column 2, lines 55-57. There is no language in the cited passages that discloses that the memory cell array of Curtis (Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) is arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. Thus, Curtis does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Curtis. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Curtis discloses the claim limitation of claims 1 and 16 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Curtis discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 1 and 16. M.P.E.P. §2131.

Appellant further asserts that Curtis does not disclose "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16. The Examiner cites column 2, lines 38-43; column 3, line 63 – column 4, line 18; and Figure 4 of Curtis as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 4. Appellant respectfully traverses.

Curtis instead discloses a packet memory system including a memory cell array having, for example, M rows by N 32 bit dynamic random access memory (DRAM) cells. Column 2, lines 38-40. Curtis further discloses a switch data flow that includes a plurality of ports. Column 3, lines 65-67. Curtis further discloses a timing diagram illustrating operation of the packet memory system of the preferred embodiment as compared to the operation of a conventional DDR II system. Column 4, lines 7-10.

There is no language in the cited passages that discloses that the memory cell array of Curtis (Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for writing selected data presented at the first one of the ports to a selected row in the array. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis

(Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined word-width during a first time period. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row during a second time period. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Appellant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row during a second time period for output at the second one of the ports. Thus, Curtis does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Curtis. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Curtis discloses the claim limitation of claims 1 and 16 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Curtis discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 1 and 16. M.P.E.P. §2131.

2. Claims 2-3 and 7 are not anticipated by Curtis for at least the reasons that claim 1 is not anticipated by Curtis.

Claims 2-3 and 7 each recite combinations of features of independent claim 1,

and thus claims 2-3 and 7 are not anticipated by Curtis for at least the reasons that claim 1 is not anticipated by Curtis.

3. Claims 20-21 are not anticipated by Curtis for at least the reasons that claim 16 is not anticipated by Curtis.

Claims 20-21 each recite combinations of features of independent claim 16, and thus claims 20-21 are not anticipated by Curtis for at least the reasons that claim 16 is not anticipated by Curtis.

4. Claims 2 and 17 are not anticipated by Curtis.

Appellant respectfully asserts that Curtis does not disclose "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17. The Examiner cites Figure 1 of Curtis as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 4. Appellant respectfully traverses and asserts that Curtis instead discloses a packet memory system including a memory cell array having, for example, M rows by N 32 bit dynamic random access memory (DRAM) cells. Column 2, lines 38-40. There is no language in Curtis that discloses a buffer associated with each port. Neither is there any language in Curtis that discloses a buffer associated with each port for converting words of data from an initial bit-width to a predetermined bit width. Thus, Curtis does not disclose all of the limitations of claims 2 and 17, and thus claims 2 and 17 are not anticipated by Curtis. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Curtis discloses the claim limitation of claims 2 and 17 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Curtis discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not

established a *prima facie* case of anticipation rejecting claims 2 and 17. M.P.E.P. §2131.

5. Claim 3 is not anticipated by Curtis.

Appellant respectfully asserts that Curtis discloses "wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead" as recited in claim 3. The Examiner cites Figure 3 of Curtis as disclosing the above-cited claim limitation. Office Action (7/26/2006), page 4. Appellant respectfully traverses. Appellant could not find any language discussing Figure 3 or any depiction in Figure 3 that discloses that the predetermined bit-width is equal to a bit-width of certain bit width and associated overhead. Thus, Curtis does not disclose all of the limitations of claim 3, and thus claim 3 is not anticipated by Curtis. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Curtis discloses the claim limitation of claim 3 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Curtis discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claim 3. M.P.E.P. §2131.

6. Claim 20 is not anticipated by Curtis.

Appellant respectfully asserts that Curtis does not disclose "wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment" as recited in claim 20. Appellant further asserts that Curtis does not disclose "where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus™, and programmable bit burst length interfaces" as recited in

claim 21 The Examiner has not specifically addressed these claim limitations. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Curtis as allegedly disclosing the claim limitations of claims 20-21, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 20-21. M.P.E.P. §2131.

In response to Appellant's above argument, the Examiner appears to simply assert that Curtis discloses the claim limitations of claims 20-21 without providing any evidence. Office Action (7/26/2006), page 8. The Examiner must provide evidence that shows that Curtis discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claims 20-21. M.P.E.P. §2131.

C. Claims 4, 9 and 18-19 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Mathur, or alternatively, over Curtis.

The Examiner rejects claims 4, 9, 18-19 under 35 U.S.C. §103(a) as being unpatentable over Mathur, or alternatively, over Curtis. Office Action (7/26/2006), page 5. Appellant respectfully traverses for at least the reasons stated below.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a

prima facie case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that neither Mathur nor Curtis teach the claim limitations of claims 4, 9, 18 and 19. Office Action (7/26/2006), page 5. However, the Examiner does not provide a motivation for modifying either Mathur or Curtis to include such limitations. The Examiner simply states:

> Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages were widely known at the time. Office Action (7/26/2006), page 6.

This (simply stating "advantages were widely known at the time") is not a motivation for modifying Mathur or Curtis to include the above-mentioned limitations. The Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mathur or Curtis to include the above-mentioned limitations. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner is instead relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Since the Examiner has not provided a motivation for modifying Mathur or Curtis to include

the above-mentioned limitations, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 4, 9, 18 and 19. *Id.*; M.P.E.P. §2143.

Further, the Examiner states:

> Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall with the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known. Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Office Action (7/26/2006), page 6.

Appellant respectfully traverses the assertion that the limitations of claims 4, 9 and 18-19 are well known. In particular, Appellant respectfully traverses the assertion that having an initial bit width of 48 bits and a predetermined bit-width of 384 bits, as recited in claim 4, is well known in the art. Appellant further traverses the assertion that having streams of data words comprising eight forty-eight bit words of ATM data and having single words having a predetermined width of 384 bits, as recited in claim 9, are well known in the art. Appellant further traverses the assertion that the selected digital format that includes an asynchronous transfer mode digital data format, as recited in claim 18, is well known in the art. Appellant further traverses the assertion that having the predetermined word-width equal a bit-width of a user data portion of an asynchronous transfer mode information packet, as recited in claim 19, is well known in the art. Appellant has requested the Examiner to provide a reference that teaches each of the above-cited claim limitations pursuant to M.P.E.P. §2144.03. However, the Examiner has never provided any such reference(s) to support the Examiner's assertions. Accordingly, the Examiner is simply relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 4, 9, 18 and 19. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

D. Claim 21 is not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Mathur.

The Examiner rejects claim 21 under 35 U.S.C. §103(a) as being unpatentable over Mathur. Office Action (7/26/2006), page 5. Appellant respectfully traverses for at least the reasons stated below.

As stated above, most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that does not teach the claim limitations of claim 21. Office Action (7/26/2006), page 5. However, the Examiner does not provide a motivation for modifying Mathur to include such limitations. The Examiner simply states:

> Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages were widely known at the time. Office Action (7/26/2006), page 6.

This (simply stating "advantages were widely known at the time") is not a motivation for modifying Mathur to include the above-mentioned limitations. The Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mathur or Curtis to include the above-mentioned limitations. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner is instead relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Since the Examiner has not provided a motivation for modifying Mathur to include the above-mentioned limitations, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 21. *Id.*; M.P.E.P. §2143.

Further, the Examiner states:

> Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall with the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known. Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Office Action (7/26/2006), page 6.

Appellant respectfully traverses the assertion that the limitations of claim 21 are well known. In particular, Appellant respectfully traverses the assertion that having a data interface selected from a group consisting of DDR, QDR, Rambus™, and programmable bit burst length interfaces, as recited in claim 21, is well known in the art. Appellant has requested the Examiner to provide a reference that teaches each of the above-cited claim limitations pursuant to M.P.E.P. §2144.03. However, the Examiner has never provided any such reference to support the Examiner's assertions. Accordingly, the Examiner is simply relying upon his own subjective opinion which

is insufficient to support a *prima facie* case of obviousness in rejecting claim 21. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-21 are in error. Appellant respectfully requests reversal of the rejections and allowance of claims 1-21.

Respectfully submitted,

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CLAIMS APPENDIX

1. A switch comprising:

a plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of said ports, said shared-memory comprising:

an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width;

circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports.

2. The switch of claim 1 and further comprising a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width.

3. The switch of claim 1 wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead.

4. The switch of claim 2 wherein said initial bit-width is 48 bits and said predetermined bit-width is 384 bits.

5. The switch of claim 1 wherein said circuitry for reading and writing comprises an available address table for storing write addresses available for selection and use in writing to selected rows said array.

6. The switch of claim 5 wherein said circuitry for reading and writing further comprises a used address table for storing addresses already used for writing data to

selected rows in said array.

7. The switch of claim 1 wherein said array comprises an array of random access memory cells of the read/write classification.

8. A shared-memory switch comprising:

a plurality of ports for exchanging data between external devices associated with each of said ports;

a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words;

a shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a said row in response to a received address;

a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; and

a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks.

9. The switch of claim 8 wherein said streams of data words comprise eight forty-eight bit words of ATM data and said single words have a said predetermined width of 384 bits.

10. The switch of claim 8 wherein each of said plurality of available address tables comprises a first-in-first-out memory.

11. The switch of claim 8 wherein each of said plurality of used address tables comprises a random access memory, that performs read and write operations.

12. The switch of claim 8 wherein each of said banks is randomly accessible.

13. The switch of claim 8 wherein each of said banks stores data corresponding to a selected said port from which data is to be read.

14. The switch of claim 8 wherein each of said banks stores data corresponding to a plurality of ports from which data is to be read in a selected order.

15. The switch of claim 8 wherein said shared-memory comprises i number of banks and said switch comprises j number of ports, where $i < j$.

16. A digital information system comprising:

first and second resources operable to exchange data in a selected digital format; and

a digital switch comprising:

first and second ports for selectively coupling said first and second resources; and

a shared memory for enabling the exchange of data between said first and second ports as words of a predetermined word-width, said shared-memory comprising:

an array of memory cells arranged as a plurality of rows and a single column having a width equal to said predetermined word-width; and

circuitry for writing a selected data word presented at said first one of said ports to a selected row in said array during a first time period and for reading said selected data word from said selected row during a second time period to

said second one of said ports.

17. The system of claim 16 wherein data are exchanged through said ports as streams of data words of an initial word-width and said switch further comprises buffers for converting data words between said initial word-width and said predetermined word-width.

18. The system of claim 16 wherein said selected digital format comprises as Asynchronous Transfer Mode digital data format.

19. The system of claim 18 wherein said predetermined word-width equals a bit-width of a user data portion of an asynchronous transfer mode information packet.

20. The system of claim 16 wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment.

21. The system of claim 16 where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), RambusTM, and programmable bit burst length interfaces.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellant in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.